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ABSTRACT OF THE DISCLOSURE

In an error and sync detection circuit, 7-bit byte data is rearranged by a data rearrangement block into 8-bit byte data where 1 byte is comprised of 8 bits. Thereafter, the 8-bit byte data is consistently used throughout the process, and each of such byte data is stored in a data storage block, which is a RAM. In a parity check block, a sync detection operation and a parity check operation are performed on the byte data from the data rearrangement block and the byte data from the data storage block, which has been Thus, the byte-to-byte conversion delayed by 1496 clocks. parallel-to-serial for a eliminates the need process serial-to-parallel conversion conversion circuit and a circuit. Use of a RAM for storing the byte data eliminates the need for a 1496-stage delay element.